

CLAIMS

What is Claimed is:

1. A method of processing an instruction, said method comprising:
fetching said instruction using a corresponding address from a memory unit,
5 wherein a plurality of possible meanings are associated with said instruction;
concatenating a portion of said corresponding address to said instruction to
form an extended instruction; and
executing said extended instruction, wherein said portion of said corresponding
address determines a meaning for said extended instruction from said possible
10 meanings.
2. The method as recited in Claim 1 wherein said portion is an address bit.
3. The method as recited in Claim 1 wherein said portion is a plurality of
15 address bits.
4. The method as recited in Claim 1 wherein said plurality of possible
meanings include an integer type of instruction and a floating point type of instruction.
- 20 5. A method of handling an instruction, said method comprising:
generating said instruction, wherein a plurality of possible meanings are
associated with said instruction;

storing said instruction at a particular address in a memory unit such that a portion of said particular address enables determination of a meaning for said instruction from said possible meanings; and

before executing said instruction, fetching said instruction using said particular address from a memory unit and concatenating said portion of said particular address to said instruction.

6. The method as recited in Claim 5 wherein said portion is an address bit.

10 7. The method as recited in Claim 5 wherein said portion is a plurality of address bits.

8. The method as recited in Claim 5 wherein said plurality of possible meanings include an integer type of instruction and a floating point type of instruction.

15

9. The method as recited in Claim 5 wherein said generating said instruction and said storing said instruction are performed by a compiler.

10. A system comprising:
20 a memory unit for storing a plurality of instructions at a plurality of addresses;

and

a processor operable to fetch a particular instruction from said memory unit by providing a corresponding address, wherein a plurality of possible meanings are

associated with said particular instruction, and wherein said processor is operable to concatenate a portion of said corresponding address to said particular instruction to determine a meaning for said particular instruction from said possible meanings before executing said particular instruction.

5

11. The system as recited in Claim 10 wherein said portion is an address bit.

12. The system as recited in Claim 10 wherein said portion is a plurality of address bits.

10

13. The system as recited in Claim 10 wherein said plurality of possible meanings include an integer type of instruction and a floating point type of instruction.

14. The system as recited in Claim 10 further comprising a compiler for
15 generating said plurality of instructions and for storing each instruction at an appropriate address in said memory unit.